

WHITEPAPER

# Low-Power Physical Design with Olympus-SoC

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**Abstract**

Reducing power consumption has become a key design challenge at 45/32 nm technology nodes. For many designs, optimizing for power is as important as timing, due to the need to reduce package cost and extend battery life. However, the complexities of designing low-power chips can negatively impact performance and time to market. Designers are being forced to juggle macro-level functional complexity issues (multiple operational modes), and micro-level process and manufacturing issues (multiple design corners) that could have conflicting power, timing, signal integrity (SI), manufacturability, and area closure requirements.

In this paper, we will explore techniques currently used in low power IC design, describe the primary challenges of low-power design, and discuss how the Olympus-SoC place and route system implements the optimal low-power solution through all steps of the physical design flow.

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## **Introduction**

One of the biggest challenges in IC design at 65 nm and below is the complexity inherent in effective power management. Whether the goal is to reduce on-chip power dissipation to reduce temperature and minimize cooling requirements, or to provide longer battery life to mobile and handheld devices, power is taking its place alongside timing as a critical dimension to be optimized during physical design. The complexity problem is exacerbated by an explosion in the number of corner, mode, and power state scenarios that could have conflicting power, timing, SI, manufacturability, and area closure requirements. The basic low-power design techniques, such as clock gating for reducing dynamic power, or multiple voltage thresholds (multi-V<sub>t</sub>) to decrease leakage current, are well-established and supported by existing tools for a single mode/corner combination. However, designers are running into difficulty with more advanced techniques, such as multi-voltage flows, designing for power in a multi-corner multi-mode context, and designing power-efficient clock trees. With a multi-voltage supply (also called multi-V<sub>dd</sub>) approach, some blocks use lower supply voltages than others, creating voltage "islands." This flow gets even more complex when dynamic voltage and frequency scaling is used to change the supply voltage level and clock frequency during operation. In designs with many corners and modes, clock power consumption depends on various factors such as the circuit design style, architectural choice, clock distribution wiring, clock driver sizing, and the capability to disable part of the clocking network using optimal clock gate placement.

As power becomes one of the major limiting factors in IC design threatening the continuation of Moore's Law, designers need new capabilities across the entire design flow that enable them to clearly see and understand the impact of power on their design. Fortunately, innovative design techniques focused on minimizing power dissipation—from high-level power-aware design and verification to back-end physical design optimization—are now emerging, enabling design teams to assess and optimize their designs. The Olympus-SoC low-power platform supports all the advanced low-power implementation techniques in a comprehensive, variability-aware place-and-route environment.

## Power Dissipation Basics

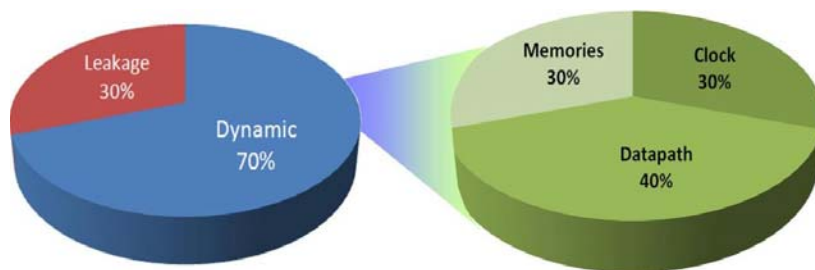
Total power consumption is a function of switching activity, capacitance, and voltage. Dynamic power, or switching power, is primarily the power dissipated when charging or discharging capacitors, as described with this formula:

$$P_{\text{dyn}} = C_L V_{\text{dd}}^2 \alpha f$$

Where

- $C_L$  is Capacitance, a function of fanout, wirelength, and transistor size.
- $V_{\text{dd}}$  is Supply Voltage, which has been dropping with successive process nodes.
- $\alpha$  is Activity Factor, meaning how often, on average, the wires switch.
- $f$  is Clock Frequency, which is increasing at each successive process node.

A typical breakdown of power dissipation at the 45 nm technology node is shown in Figure 1.



*Figure 1. Power dissipation profile at 45 nm. The total power dissipation is shown on the left. The breakdown of the dynamic power usage is illustrated on the right.*

Static power, or leakage power, is a function of the supply voltage ( $V_{\text{dd}}$ ), the switching threshold ( $V_t$ ), and transistor sizes. As process nodes shrink, leakage becomes a more significant source of energy use, consuming at least 30 percent of total power at the 65 nm technology node [J. Kao, et al. 2002]. Crowbar currents, caused when both the PMOS and NMOS devices are simultaneously on, also contribute to the leakage power dissipation. The quadratic dependency of leakage power on total transistor count easily qualifies leakage optimization as a key design objective.

## **Low-Power Challenges in Physical Design**

The challenge of low-power physical design is to create, optimize, and verify the physical layout so that it meets the power budget along with traditional timing, SI, performance, and area goals. The design tool must find the best tradeoffs when implementing any number of low-power techniques.

While low-power design starts at the architectural level, the low-power design techniques continue through place and route. Physical design tools must interpret the power intent and implement the layout correctly, from placement of special cells to routing and optimization across power domains in the presence of multiple corners, modes, and power states, plus manufacturing variability. While many tools support the more common low-power techniques, such as clock gating, designers run into difficulty with more advanced techniques, such as the use of multiple voltage domains, which cause the design size and complexity to explode.

### **Multi-voltage, Multi-corner, Multi-mode Designs**

An increasingly common technique to reduce power is the use of multiple voltage islands (domains), which allows some blocks to use lower supply voltages than others, or to be completely shut off for certain modes of operation. Multi-voltage designs are difficult to implement because of the different voltage levels used for different blocks, and the need to handle special cells such as level shifters and isolation cells. These design styles also cause the number of modes and corners to increase significantly when min/max voltage combinations from all the power domains are considered. Because each different voltage supply and operational mode implies different timing and power constraints on the design, multi-voltage methodologies cause the number of design corners to increase exponentially with the addition of each domain or voltage island. Additionally, the worst-case power corners don't necessarily correspond to the worst-case timing, so it's virtually impossible to know how to pick a set of corners that will result in true optimization across all design objectives without excessive design margins. Figure 2 shows how the corners and power states proliferate for even a simple multi-voltage design. The core operates at 1.2V or 1.8V.

One power island operates at 0.9-1.2V and can switch on and off. The second power island operates at 0.9-1.5V.

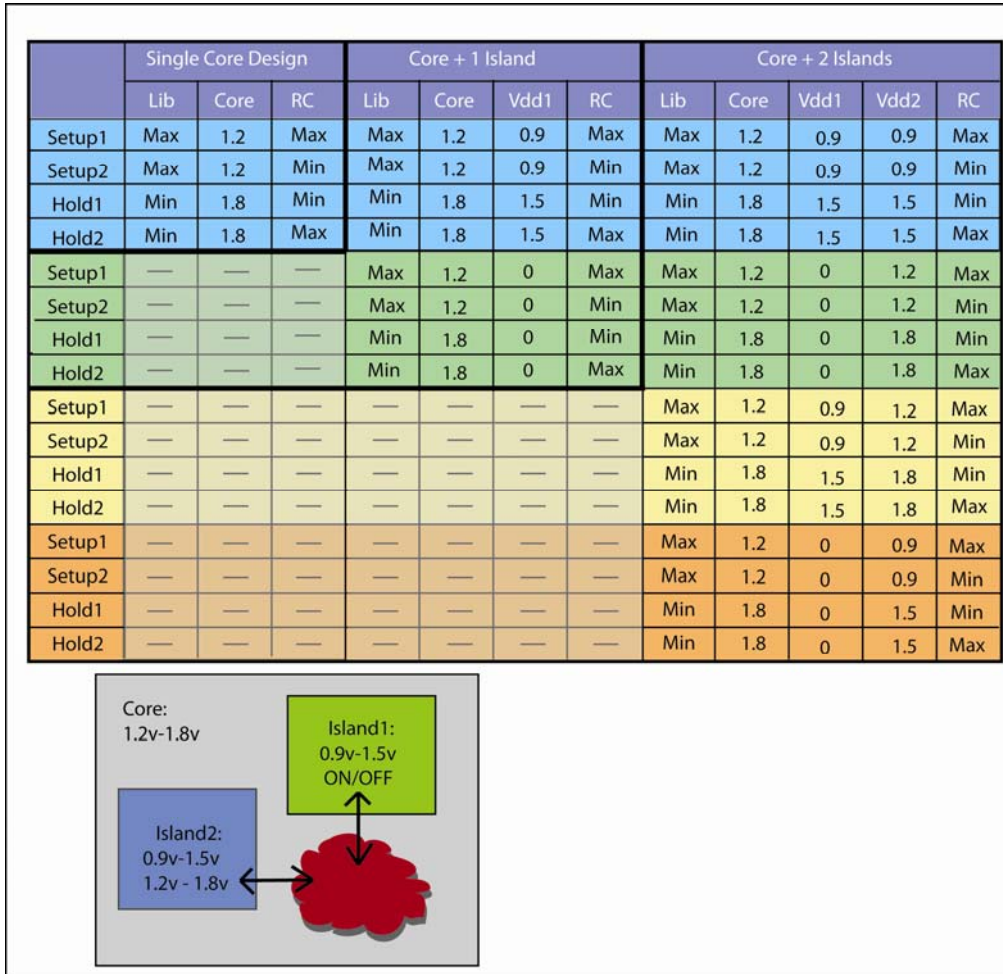


Figure 2: Each additional power domain adds to the corners under which the design needs to be optimized and verified.

To close the design across all modes, corners, and power domains, the setup and hold times must be analyzed simultaneously for different combinations of library models, voltages, and interconnect (RC) corners. Incumbent implementation flows are designed to handle one or two scenarios and are not well-suited for solving power and timing constraints concurrently. Each timing and optimization iteration would require multiple RC extractions, timing analysis runs, and power analysis runs, which increases the engineering effort during the final stages

of the chip implementation. This leads to unpredictability in sign-off ECO loops, and added margins that reduce design performance, increase power dissipation and design area, and lower yields.

This approach offers no guarantee of convergence because optimizations in one scenario could create a new violation in a different scenario. Not surprisingly, taking this limited approach, coupled with late-stage unpredictability, is resulting in less-than-acceptable power performance, higher chip failures and overall delayed schedules. The only reasonable solution is to analyze and optimize the design for all corners and modes concurrently. In other words, low-power design inherently requires concurrent multi-corner, multi-mode (MCMM) optimization for power, timing, SI, manufacturability, and die area.

## **Clock Tree Synthesis**

Clocks are a significant source of dynamic power usage, and clock tree synthesis (CTS) and optimization is a good place to achieve power saving in physical design. Low-power CTS strategies include lowering overall capacitance and minimizing switching activity, both of which are discussed below. However, getting the best power results from CTS depends on the ability to synthesize the clocks for multiple corners and modes concurrently in the presence of design and manufacturing variability, and in multi-voltage flows. Advanced gating techniques also help optimize clock power, and the physical placement of clock gates should be considered with both timing and power cost functions.

Clocks present additional challenges at advanced nodes because of the sharp increases in resistance that comes with the smaller geometries. Variation in resistance is also increasing as the wires become more sensitive to manufacturing variations in wire dimensions. Figure 3 illustrates the increases in resistance and the growing variations in resistance from 90 nm to 45 nm processes.

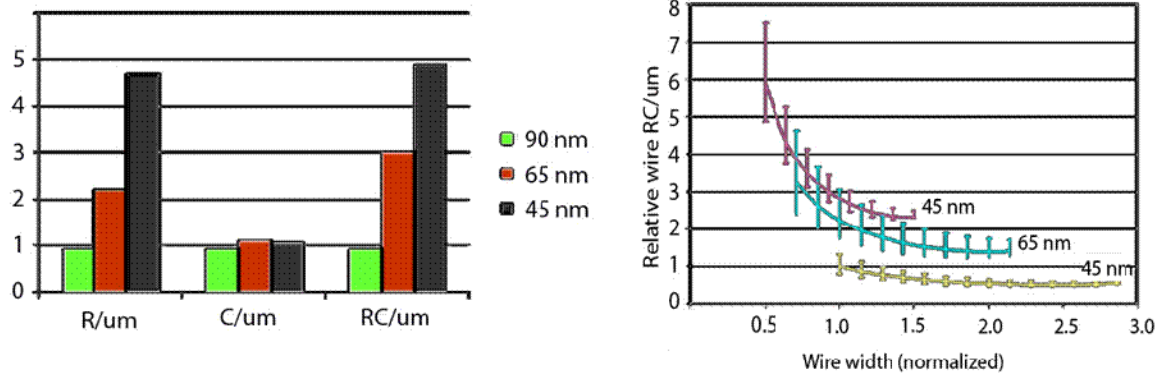


Figure 3. Resistance, shown on the left, and variations in resistance, shown on the right, increase dramatically with shrinking process nodes. These phenomena lead to the growing challenge of balancing clock skew across multiple corners.

## Increase in Functionality and Design Size

Tool capacity is also an important factor in the validity of power closure. Large designs of 100 million gates or more pack more functionality on a single chip, especially for mobile applications. Depending on the capacity of the place and route tool, designers are forced to implement the design piecemeal, never able to see all the information in context at once. This is of particular concern when optimizing for timing and power in a full-chip context, and when a designer wants to consider multiple corners and modes concurrently.

## Low-Power Implementation with Olympus-SoC

The Olympus-SoC low-power platform comprehensively handles the requirements of low-power design, while ensuring optimization of the overall solution without excessive design iterations, enabling engineers to rapidly deliver fully-optimized, power-efficient designs. The Olympus-SoC low-power platform has a number of capabilities to manage both design intent and total power optimization, and to make intelligent tradeoffs between power, area, and timing across all the corners and modes throughout the design flow. Olympus-SoC is well suited for low-power designs because its MCM analysis drives closure for all design modes, process corners, and power constraints simultaneously. The Olympus-SoC low-power

platform includes the following key technologies to address low-power challenges and deliver best quality of results:

- Completely automated multi-voltage flow with support for Dynamic Voltage and Frequency Scaling (DVFS) to handle varying supply voltages and clock frequencies, and the capability to handle special cells such as level shifters, isolation cells, and multi-threshold CMOS (MTCMOS) switches.
- Power-aware CTS with smart clock gate placement, slew shaping, register clumping, and concurrent MCMM optimization that ensures a balanced clock tree with the minimum number of clock buffers.
- Unique architecture that provides seamless concurrent optimization for both power and timing, covering all operating modes and corners through all stages of the flow.
- Unified Power Format (UPF)-based Netlist-to-GDSII flow, including support for power state tables.

Additionally, Olympus-SoC offers techniques such as concurrent multi-Vt optimization, power gating, retention flop synthesis, gas station methodology, and power-aware buffering and sizing. Olympus-SoC customers are experiencing 2-3X faster design closure times, and up to 30% power savings versus traditional tools.

The Olympus-SoC system is architected for handling large, complex, low-power SoCs with the ability to handle 100 million+ gates in flat mode. Fully-multithreaded analysis engines and the industry's only fully-parallelized timing and optimization engine provide up to 7X speed-up on multi-core and multi-CPU computing platforms.

## **Multi-Voltage Flow with Olympus-SoC**

Multi-voltage design, a mainstream technique to reduce total power, is a complex, time-consuming task, because many blocks are operating at different voltages, or intermittently shut off. Level shifter and isolation cells need to be used on nets that cross domain boundaries if the supply voltages are different, or if one of the blocks is being shut down. DVFS is an



extension of the multi-voltage flow where the supply voltage and frequency can vary dynamically. Power gating using MTCMOS switches involves switching off certain portions of an IC when that functionality is not required, then restoring power when that functionality is needed. Gas station methodology is used in conjunction with the multi-voltage flow to effectively handle top-level nets that are routed over voltage islands. Designers also use retention memory elements to retain key state data during the sleep mode, so it can be correctly restored upon power up.

Olympus-SoC is UPF-compliant, so the power intent for multi-voltage design, which is described in the UPF file, is carried through the physical design flow. Each step of the flow offers opportunities for power savings through clever implementation techniques, some of which are described in the following sections. Figure 4 illustrates the netlist-to-GDSII multi-voltage flow in Olympus-SoC.

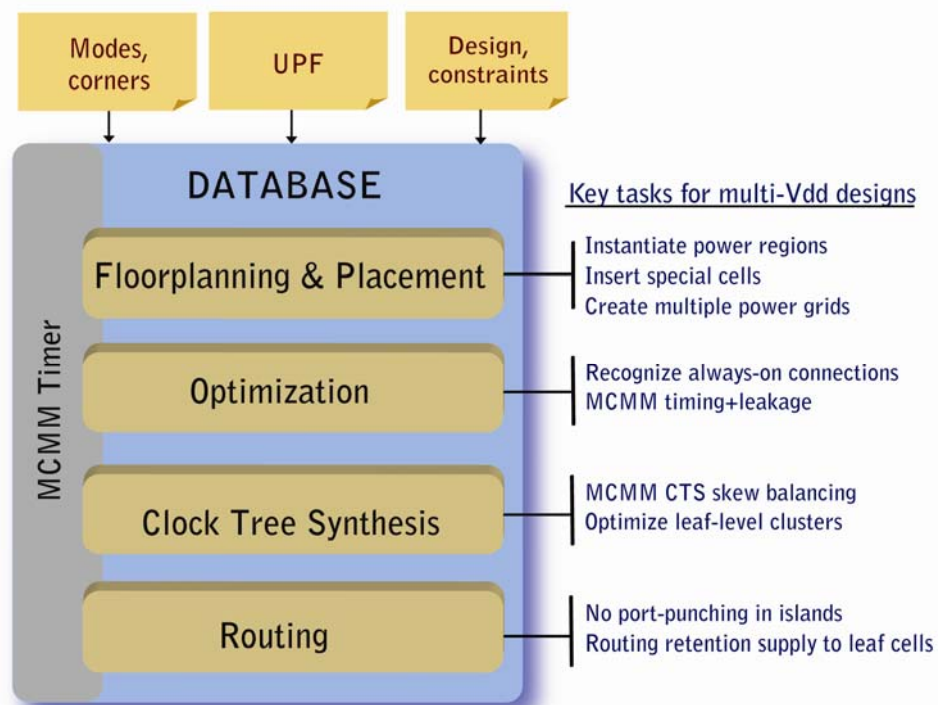


Figure 4. Physical design flow for multi-voltage designs includes the ability to define power domains in Unified Power Format (UPF), and advanced features for placing and routing across domains and for optimizing clock trees for all operating modes.

A little extra time spent in capturing the power intent in UPF can pay off by avoiding implementation and verifications problems later in the flow. After reading in the power specifications, designers can analyze domains and power connectivity with queries to the Olympus-SoC database. Olympus-SoC can trace connectivity on power pins just like on signal pins, verify the power applied to a given pin, and check isolation cells, level shifters, switches, and retention cells. The UPF file includes the power state table (PST), which defines the combinations of voltages and power states that are essentially treated as operational modes in the Olympus-SoC MCMM environment.

Domain definition and supply net information from the UPF file is used during the floorplanning stage, the first step in the flow. During floorplanning, physical domains are created and the corresponding power structure is created for each individual supply net defined in the UPF file. Domain-specific hierarchy mapping and library association are defined by the user based on the architecture.

Also during floorplanning, the native row-cutter identifies legal rows in different voltage islands, and places IO pads to provide the initial guides for cell placement. The Olympus-SoC numerical prototyping placer then groups cells into partitions, and assigns partition pins. Designers can control the placement of isolation cells and level shifters by specifying regions and net-weights. Even with no specific UPF directives, Olympus-SoC places cells on the most active nets closer to each other? to minimize switching power. To verify the power domain setup, Olympus-SoC analyzes level shifters and isolation cells to ensure they are correctly placed before proceeding with routing. It will also check always-on connections to ensure that the signal is not lost due to OFF state voltage islands.

### ***Using MTCMOS Switches***

Power gating to shut down certain blocks using MTCMOS switches to minimize leakage power is done within the Olympus-SoC multi-voltage infrastructure. Domains that need to be powered down are captured in the UPF file, along with the switch and the enable line definition. The switch is connected between the constant supply and the variable supply and is controlled using the switch enable line. Olympus-SoC uses several different approaches for switch cell insertion, including peripheral, distributed, and fine grain insertion, to facilitate

implementation for different design styles. Figure 5 illustrates the distributed-style switch cell methodology.

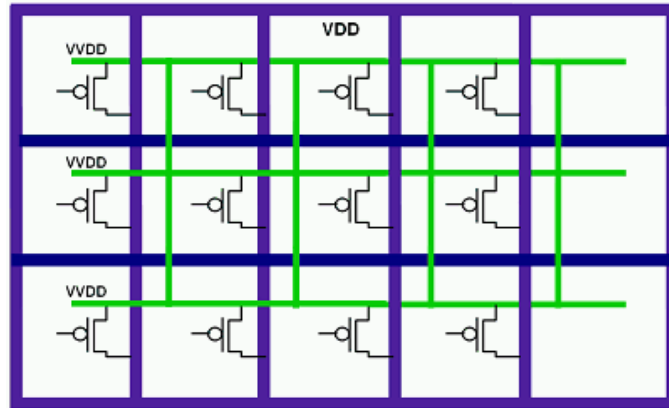


Figure 5. Distributed PMOS switch cell insertion methodology.

Domains that are powered down using switch cells should also have isolation cells for any nets that cross the domain (to eliminate floating nets). Olympus-SoC automatically handles both level shifters and isolation cells when there is a difference in supply voltage. Special sequential elements are also needed to retain state when the block is powered down. Inserting and hooking up retention flops is done automatically by Olympus-SoC if the flops are present in the incoming netlist. When stitching the enable lines for the switches, care must be taken to minimize rush currents when the block is powered on. Olympus-SoC provides a flexible API that allows designers to customize enable line stitching to minimize switching transients.

Another key consideration for multi-voltage flows is top-level net buffering. Nets that cross multiple domains need special always-on buffers when passing through domains that are powered down. Olympus-SoC supports the “gas station” methodology to handle top-level nets while minimizing area and power. Always-on buffer insertion is also supported for enable line buffering of switch cells.

The CTS engine and the router honor domain boundaries, and will be discussed in detail in the following sections. Every domain has its own clock tree network with one entry point. Level shifters are inserted automatically on the clock if there is a difference in voltage levels

between domains. By default, Olympus-SoC honors domain boundaries and contains routes within the domains.

## Power-Aware Clock Tree Synthesis

Because clocks are a large source of dynamic power usage, no low-power design strategy would be complete without serious attention to the clock tree. Olympus-SoC has several key capabilities for optimizing clock trees for low power:

- Reducing functional skew and skew across corners with MCMM CTS
- Lowering leaf cluster capacitance with register clumping and clock gate cloning and de-cloning
- Improving clock gating coverage with netlist-level gating
- Minimizing switching activity with smart clock gate placement

Concurrent MCMM CTS allows dynamic tradeoffs among all corner/mode and power state scenarios simultaneously. The experiences of customers using MCMM CTS show significant reduction in area, number of buffers, skew, total negative slack (TNS) and worst negative slack (WNS), in addition to lower dynamic power. The example in Figure 6 shows how, for a given mode, a single-corner CTS implementation compares with a 9-corner CTS implementation for a 9-corner design.

QOR METRIC	One Corner CTS	Multi-corner CTS (9 corners)	Improvement
Clock Skew (across corners)	145	87	<b>40%</b>
Hold Buffer Area	7816	3598	<b>54%</b>
Total Area	18968	15622	<b>18%</b>
TNS	-32056	-28722	<b>10%</b>
WNS	-127	-122	<b>4%</b>

Figure 6: CTS with Olympus-SoC — MCMM vs. single-corner.

Most CTS tools balance global skew across all the flops, regardless of which level of the clock tree they inhabit. Designers then have to manually drive CTS to balance the sinks correctly. Olympus-SoC analyzes flop interactions to derive the exact skew balancing requirements at the different clock tree levels, and across different voltage islands. The result is better buffer count, lower wire length, and lower power. It also simplifies CTS setup because there is no need to manually direct functional skew balancing.

### **Lowering Leaf Cluster Capacitance**

Because the leaf clusters (wire and pins) carry most capacitance in the clock tree, having dynamically updated RC calculation during CTS allows for leaf clustering that minimizes capacitance, and therefore reduces power. Olympus-SoC calls on-the-fly global routing during clock buffer insertion so that the CTS engine sees more accurate topology, and it also uses an incremental, on-the-fly fast extraction during CTS for dynamic, accurate and fast parasitics and delay calculation. Olympus-SoC also clumps registers during placement to minimize capacitance on the clock tree network.

### **Minimizing Clock Switching with Clock Gating**

Clock gating is a common technique for reducing clock power by shutting off the clock to unused sinks. Olympus-SoC performs netlist-level clock gating to improve clock gating coverage. Olympus-SoC does this with clock restructuring, a post-CTS optimization technique that identifies missed clock gating opportunities. It analyzes enable functions, identifies common sub-terms and intelligently determines the optimal number of gates that still meet setup constraints, introducing new gates upstream as needed. Olympus-SoC makes dynamic tradeoffs between clock gate placements based on power consumption, which is a factor of capacitance, switching activity, and wire length.

As illustrated in Figure 7, if the probability of switching is equal on both sides of a clock gate, CTS can balance the tree for the best buffer count and lowest wire length. If the toggle rates on either side of a clock gate are different, CTS will minimize the wire length on the high-frequency wires to lower power, even at the expense of higher buffer count or wire length.

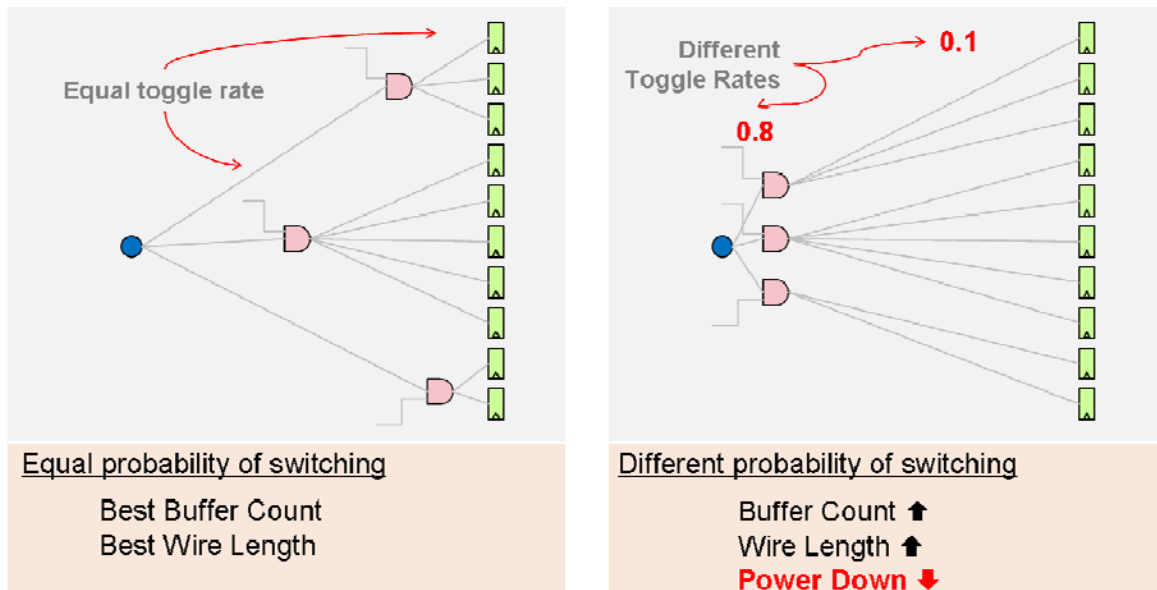


Figure 7: Tradeoffs in clock gate placement for lower power.

Along with power-aware clock gate placement, Olympus-SoC also automatically performs clock gate cloning and de-cloning to optimize and balance the load on the clock tree network.

## Power-aware Routing

During all routing stages, Olympus-SoC follows the power intent as specified in the UPF file. This includes maintaining a single port of entry for boundary nets, and respecting voltage island boundaries. The router handles secondary power connections for retention flip-flops, level shifters, and always-on buffers. It obeys voltage islands by default, and will change routing topology to meet other design constraints. For example, it will detour around an island to buffer an SI violation on a non-critical net, but allow critical nets to cross an island. For finer control of multi-voltage routing, users can add a property to nets that keeps them exclusively inside or outside of a voltage island.

The router gets constant updates on MCM timing and RC, which it uses to find the optimal solution for meeting power, timing, SI, manufacturability, and area constraints. The advanced router is DFM-aware so it “sees” and accounts for the manufacturing issues that affect power (especially leakage power), such as variations in on-chip temperature and thickness.

## **Concurrent MCMM Power and Timing Optimization**

MCMM timing analysis and optimization is the heart of the Olympus-SoC system and is performed throughout the flow. After routing, the power of MCMM in making the final trade-offs to achieve the power, timing, SI, manufacturability, and area goals are evident as a key value in the Olympus-SoC flow. The optimizations that benefit from MCMM include replacing low- Vt cells with high-Vt cells, which reduces the leakage power. High-Vt cells can increase delay, so it is crucial to have an accurate MCMM timing engine determining which paths can tolerate high-Vt cells and still meet timing under all corner/mode scenarios.

## **Summary**

Reducing power consumption has become a key design challenge at advanced technology nodes. For many IC designs, optimizing for power is as important as timing, due to the need to reduce package cost and extend battery life. Olympus-SoC offers comprehensive power closure capabilities with three key technologies: MCMM optimization, support for multi-voltage designs, and advanced low power CTS.

Olympus-SoC is the only place-and-route system to offer true concurrent MCMM power and timing closure for optimal quality of results and fast turnaround time. With full support of UPF commands, Olympus-SoC handles multi-voltage design requirements through the entire place-and-route flow. It automates the placement of level shifters, isolation cells, and MTCMOS switches, and provides complete graphical analysis, optimization, and verification of power domain cells and connectivity. Finally, the advanced CTS and clock optimization techniques are extremely effective at lowering clock power. These capabilities remove the unpredictability from the physical implementation process, which affect the cost, performance, and time-to-market of low-power ICs.

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